MAGNETIC-CORE LOGIC FOR DIGITAL COMPUTORS

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THESIS

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FOR
DIGITAL COMPUTERS

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PREFACE

The increasing use of digital computers, both individually and as units of systems, and their inherent complexity has led to considerable effort toward improving their reliability. With this in mind, a project was undertaken to investigate the feasibility of using magnetic cores instead of vacuum tubes in the arithmetic unit of such computers. This involved the design and testing of a magnetic-core shift register and circuits to implement the logical OR and NOT operations with cores. Using these as a basis, various logical designs for an adder were investigated. The design of a simple all-core arithmetic unit is presented and compared with its vacuum tube equivalent.

Most of the work described was done during the period from January 3 to March 18, 1955, at International Telemeter Corporation in Los Angeles. The author is especially indebted to Dr. Louis N. Ridenour, Mr. Milton Rosenberg, and Mr. Witold Modlinski for their cooperation and helpful suggestions during this period.

TABLE OF CONTENTS

Item	Title	Page
Chapter I	Introduction	1
Chapter II	Magnetic Materials	5
Chapter III	Systems Considerations and Comparisons	10
Chapter IV	Test Equipment	13
Chapter V	Design of Shift Register and Logical Circuits	15
Chapter VI	Adder Design	23
Chapter VII	Experimental Results	27
Chapter VIII	Conclusions, Recommendations, and Possibilities	34
Illustrations	. . . .	40
Bibliography	. . . .	50
Appendix I	Binary Logic	52

LIST OF ILLUSTRATIONS

Figure Page

1. Voltage output from switched core 40
2. Idealized slant hysteresis loop 40
3. Operating conditions on slant-loop core . 40
4. Proposed magnetic-core arithmetic unit . . 41
5. Basic form of one-core-per-bit shift register 41
6. Basic form of two-cores-per-bit shift register 41
7. Idealized square hysteresis loop of ferrite core 42
8. Time relationship of "A" and "B" shift pulses 42
9. Logical OR circuit 42
10. Logical NOT circuit 43
11. Three-input adder 43
12. Relationships existing in three-input adder of Figure 11 44
13. Truth table 44
14. Block diagram of modified half-adder . . . 44
15. Block diagram of full adder 45
16. Shift register output pulse 45
17. Current pulse conditions in complementing circuit 45
18. Schematic diagram of modified half-adder 46
19. Block diagram of buffered half-adder . . . 46

Figure Page

20. Block diagram of computer arithmetic unit using magnetic cores 47

21. Function table for comparison of X and Y 48

22. Various forms of logical equations . . . 49

LIST OF ABBREVIATIONS AND SYMBOLS

mmf	Magnetomotive force
NI	Ampere-turns
S/N	Signal-to-noise ratio
H_c	Coercive force or coercivity
B_r	Residual flux density
B_s	Saturation flux density
μsec	Microseconds
DC	Direct current
Kc	Kilocycles
ma	Milliamperes
H_m	Applied magnetic field strength

CHAPTER I

INTRODUCTION

In the field of electronic computers of the digital variety any physical device which exhibits two or more stable states may be used to store information.[1] Various types of vaccum tube flip-flops have been used in this manner for many years. Shortly after World War II with the advent of metals, and later ferrites, which were characterized by relatively square hysteresis loops a new field of bistable devices became available to scientists and engineers. In general it was found convenient to form the magnetic core material in the shape of a toroid. In the case of the metals such as Deltamax and 4-79 Mo-Permalloy the metal was rolled into a thin strip which was generally wound on a ceramic bobbin, proper precautions being taken to insulate one turn from the next. The ferromagnetic ferrites were molded or pressed into the desired toroidal form, then sintered.

The information storage is achieved by pulsing a winding which links the core with a current of magnitude sufficient to cause the flux to reach a maximum along a major hysteresis loop, either in a positive or negative direction depending upon the sense of the drive winding. When the

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[1] Since most common storage devices presently in use are restricted to two stable states the discussion which follows will be confined to bistable devices.

current pulse is removed the core returns along the loop to its remanent state of magnetization and remains there in the absence of further excitation. This magnetizing process may be carried out by providing the net mmf necessary to saturate the core by supplying current through more than one winding simultaneously. This technique leads to the familiar type of coincident-current magnetic-core matrix memory which has gained considerable prominence among computer storage systems in recent years as a result of its high reliability, high-speed random-access feature, good S/N, potentially low cost per bit and high density storage capacity. Such a memory consisting of 4096 words, each 40 bits long, was recently delivered to the Rand Corporation by International Telemeter Corporation.

Another computer application for which magnetic cores have recently been adopted is that of static delay lines or shift registers in which information is propagated down a series of cores, literally bit by bit. The method by which this is accomplished utilizes the storage properties of the core during part of the cycle and later the ability of the core to act as a transformer in passing the stored information to the following core. Inherent in such a gating operation are the possibilities of performing logical arithmetic operations on the stored digits, either serially or in parallel. The purpose of the present investigation is to determine the feasibility of using magnetic cores to perform the logical operations normally handled by vacuum tubes.

The advantages are obvious. The reliability of cores is exceedingly high. They are not subject to injury due to accidental electrical overloads on the circuit. No deterioration in the size or squareness of the hysteresis loop has been noted as a function of aging. Once installed, maintenance is virtually unnecessary and, in fact, is limited to the associated circuitry and connections, none is necessary for the magnetic elements themselves. Although some power is required to shift the information along, none is required to store it and a power failure does not destroy the pattern stored. With filament heaters eliminated the power requirements are reduced appreciably. The price of a switch core is at present in the order of a dollar or less, most of this due to the cost of testing and grading and there is good reason to believe that mass production can be expected to reduce the cost to about a tenth of this figure. The numerical relationship between cores and tubes in performing computing functions is difficult to establish generally, but seems to run about one to one. Although at present the current pulses used to drive the cores are generally formed by vacuum tubes, techniques common to pulse radar could be used to relegate this function, too, to magnetic cores or saturable reactors. The concept, then, of an electronic computer devoid of vacuum tubes or transistors is not unthinkable.

The purpose of this thesis was to investigate the various implications of such a system including the properties

of the magnetic components themselves, the associated circuitry both from a logical design basis and electronic design practice, and the entire systems concept.

The design, construction, and testing of a magnetic-core shift register are described. The various logical operations of binary arithmetic are investigated from the standpoint of cores and circuits are described which were successfully used to perform these operations. Two types of adders are discussed and the relative advantages and practical difficulties of each are considered. Finally, further possibilities in the field of magnetic core logic are indicated.

It is concluded that an all-core, i.e., no vacuum tubes or transistors, computing system is completely feasible and the design of a simple system of this type is presented. The timing problems which occur in the logical portion of the system impose some degree of limitation upon the speed with which the remainder of the system might theoretically operate, however, this restriction appears not to be too serious.

The experimental results of this investigation, together with an analysis based on these results, indicate the types of logical operations which may be performed with cores, the speed that may be obtained, the power requirements, and the timing conditions that must be met. It is shown that magnetic-core logic of the type discussed offers the advantages of environmental ruggedness, general reliability, and economy of size and power in systems operating below approximately 100 Kc.

CHAPTER II

MAGNETIC MATERIALS

The recent widespread adoption of magnetic elements as digital computer components has stimulated considerable research in magnetic materials. For most computer applications the desirable characteristics of a magnetic material are a relatively square hysteresis loop, a short switching time, and a low coercive force. In addition, the cores should be easily manufactured in large quantities with a high degree of uniformity.

Although this paper is written from an engineering viewpoint, it seems desirable to include at this point a brief summary of some of the physicists' basic theory of the flux-reversal mechanism in polycrystalline materials. Much work in this field has been done recently by Goodenough [3,4], Menyuk [3], Kittel [6], Bozorth [1] and others.

The latest theory of magnetization assumes that the magnetic material is composed of a number of small regions called domains, within each of which the local magnetization is saturated. The direction of magnetization of the various domains need not necessarily be parallel however.

According to this domain theory of magnetization the reversal of induction in a core results chiefly from the nucleation of domains of reverse magnetization and motion of the 180° Bloch walls which separate the growing domains. The centers of nucleation from which the domains of reverse mag-

netization first grow occur at lattice imperfections which are, in most cases, grain boundaries. The squareness of the hysteresis loop depends on the degree of alignment of the axes of easy magnetization in the individual grains. For this reason treatments such as magnetic anneal, grain orientation, and the application of mechanical stress are commonly used to further this alignment.

The switching time necessary for a complete flux reversal within the core is directly related to the velocity of the domain wall movement. This velocity is in turn limited by a viscous damping term which is composed of two factors. The first is a function of eddy currents and is negligible in either ultra-thin metal tapes (of the order of 1/8 mil) or in the ferrites which have resistivities of about 10^6 ohm-cm which is some 10^{12} times that of the metals. The second factor is the relaxation contribution which arises from the delayed response of the electron spin vectors in aligning themselves in the direction of the applied field.

A switching coefficient, S_w, has been defined as:

$$S_w = (H_m - H_o)\tau$$

where H_m is the applied field

H_o is the threshold field for irreversible domain wall motion

and τ is the switching time.

For a given material S_w is essentially constant for $H_m > 2H_o$ implying the inverse relationship of τ and the applied field.

S_w for metal cores is about half that for the ferrites. Since, however, H_m is limited to about $2H_c$ for coincident current memory applications, ferrite cores switch faster solely by virtue of their higher coercivity. This fact, coupled with the large number of cores usually needed for practical memory applications, has lead to the almost exclusive use of ferrite cores in memories. The S-1 ferrite material now being used has a nominal switching time of about one µsec.

The mechanisms of domain wall movement may be used to explain the output voltage waveforms observed when a core is switched under various conditions. For instance, if a core is driven by a field only slightly greater than the coercive force a voltage output similar to that shown in Figure 1 may be observed. The first maximum is attributed to domain creation and reversible wall motion and its rise time appears to be limited only by the rise time of the driving current pulse. The second maximum, which occurs only when $H_m > H_c$, is thought to be due to the irreversible wall motion of many growing domains. This second maximum tends to increase in amplitude and occur sooner as H_m is increased until eventually it blends into the first and its identity is lost.

By reducing the grain size more nucleating centers are created and the switching time is speeded up; however, this reduction in grain size also tends to increase the coercivity, hence for any given material and application an optimum grain size exists.

A high Curie point is desirable both to reduce the relaxation losses and to permit more stable operation at higher pulse rates where heat dissipation may become a serious problem. The metal cores may be cooled without too much difficulty but because of the poor heat conductivity of the ferrites attempts to cool them succeed only in setting up a temperature gradient within the core. A representative Curie temperature for metals is about 460° Centigrade and for ferrites about 300° Centigrade. This, and the fact that metals usually have lower coercivities and higher flux densities than the ferrites, has favored the use of metal cores in shift registers and switching circuits.

Work being done at the Naval Ordnance Laboratory, Corona, on the evaporation of thin magnetic films gives promise of very fast switching times [8].

It may be well to note at this point that the square hysteresis loop mentioned in the previous discussion is not the only one which can be used for logical operations with cores. A material having hysteresis characteristics which may be idealized as shown in Figure 2 may also be used for gating operations. Ferramic I, one of the ferrites which most closely approximates this ideal, has the following nominal characteristics:

$B_s = 1510$ gauss
$B_r = 725$ gauss
$H_c = .24$ oersteds

The gating operation of such cores may be explained by referring to Figure 3. A DC bias current, when present, moves

the operating point near saturation, hence any unipolar signal impressed on an input winding will produce little change of flux and little output. Without the bias the core returns to its remanent state and traverses a minor loop determined by the amplitude of the input signal. The flux change for this operation may be many times that which occurred up on the flat portion of the loop and a usable S/N can be realized in this way when only a voltage signal is required.

By confining operation to a minor loop the disadvantages due to the heating effects of high pulse rates and the slower switching times often associated with ferrites are minimized.

CHAPTER III

SYSTEMS CONSIDERATIONS AND COMPARISONS

If magnetic cores are to be adopted for extensive use in the arithmetic units of computers they must stand on their merits in competition against the devices now in use for such purposes, specifically vacuum tubes. This indicates the desirability of a comparison of cores with tubes on the basis of pertinent operating characteristics.

1. Speed

Cores of S-1 material have a nominal turnover time of about one µsec as pointed out in Chapter II. Faster operation can be realized in other than coincident current applications by increasing the driving mmf, but power dissipation at high pulse rates soon becomes a problem, especially with the ferrites which are poor heat conductors.

In vacuum tube circuits, especially in applications as adders, a tube may perform its designated function immediately upon receipt of the information from the preceding stage. In cores, which are basically passive elements, the operation must normally wait for the arrival of a clock or shift pulse to supply the necessary power for transfer to the succeeding stage.

In general, then, core operation will be slower than tubes, but by a factor of less than ten.

2. Power

The power required from the source during switching of

a core which is driving another similar core has been shown to be [14]:

$$P_s = 4F_sV_t \qquad (1)$$

where F_s is NI required to switch a core in time T if it has no load

V_t is the output voltage per turn when a core is switched in time T.

Experimental data on the cores used in this investigation showed that about 2.3 NI was required to switch an unloaded core in five µsec with an output of about ¼ volt per turn. Substituting these values in (1),

$$P_s = 4\text{x}2.3\text{x}\tfrac{1}{4} = 2.3 \text{ watts}$$

which represents an energy loss of

$$P_sT = 2.3\text{x}5\text{x}10^{-6} = 11.5 \text{ microjoules per pulse,}$$

or, for 50 Kc operation, a power dissipation of .575 watts. This is substantially less than that sustained by a normal computer type tube in standby condition, i.e., filament heaters on, without considering any losses from the plate supply necessary for the transfer of information.

3. Reliability

Although cores have been in use for a period of several years the literature records no instance of the direct failure of a magnetic element but, of course, the associated electronic circuitry is subject to the same limitations as in other applications. No gradual deterioration in performance comparable to low emission in vacuum tubes is encountered.

Perhaps the weakest link, from the standpoint of reliability, in the computing system outlined in this paper is in the use of semi-conductor diodes. Recent manufacturing improvements are claimed to have pushed the life expectancy of such units above 20,000 hours.

On the other hand, premium quality computer tubes are guaranteed for only 10,000 hours in most cases although conservative circuit design and operation at reduced ratings have pushed the actual life beyond this figure in some cases.

4. Cost

The present cost of graded switch cores is in the order of one dollar but quantity production and increased automation in processing and grading should reduce this figure by a factor of ten.

Premium tubes of the type mentioned above are somewhat more expensive than this.

5. General

To fully investigate all the ramifications and potentialities of using magnetic cores in digital computers the system in Figure 4 was chosen as a representative problem. It was felt that if such a system could be designed in some detail and, if possible, built and operated, using no vacuum tubes or transistors it would embody most of the essential features common to modern electronic computers and would, in fact, constitute in itself a simple computing system which could conceivably be expanded into as complex a system as desired. The logical arrangement is a representative basic arithmetic unit in itself.

CHAPTER IV

TEST EQUIPMENT

The testing of the various circuits described in this paper was greatly facilitated by the Magnetic Circuit Tester developed by International Telemeter Corporation. This versatile piece of test equipment provides four current pulse drivers, two positive and two negative, which are independently variable in amplitude from 50 to 800 ma. An eight step program is available, each of the eight "slots" being 50 µsec long and separated by 50 µsec from the next. Either one or neither of two pulses, designated P1 and P2, may be programmed into each slot. P1 is variable in duration from ½ to 40 µsec and commences near the leading edge of the slot. P2 is also variable from ½ to 40 µsec and may be positioned at any point within the slot. As an additional refinement it is possible to alter the program to recycle the last two slots either zero, six, or 20 extra times per cycle. This is invaluable for observing flux build-up under certain marginal operating conditions. Synchronizing pulses are available at an output terminal to enable the user to observe waveforms in any specified one of the eight slots, or the output of all eight may be presented simultaneously on eight successive sweeps of the oscilloscope.

Before leaving the test equipment it may be well to discuss some of the terminology used in making the tests.

Operating characteristics inherent in the type of

magnetic circuits used, and further discussed in the next chapter, lead to the convention of representing a binary "0" by the absence of a pulse and a "1" by the presence of a pulse. Following the terminology of switch-core circuits these can be identified on the basis of their respective origins as "disturbed" signals and "turnover" signals. A further distinction can be made on the basis of their desirability at a given point in the system as "unwanted" or "wanted" and it is a short step from here to the familiar concept of signal-to-noise ratio, S/N. Furthermore, since the time integral of the observed voltage waveforms is a measure of the total flux change and since an all-core system is basically dependent on the efficiency of an operation which can be thought of as flux transfer between stages, this area is a more significant parameter than is the amplitude of the output signal. For this reason the S/N as used in this paper will refer to the ratio of the "wanted" to the "unwanted" signal on an area basis.

It is to be noted that in systems requiring a transition from magnetic to electronic devices, where relative flux areas are not important, it is possible to take advantage of further integration techniques or to "strobe" (sample) the output at a time after the disturbed signal has died away but while the turnover signal is near its maximum. Signal-to-noise ratios obtained under these conditions may be very high.

CHAPTER V

DESIGN OF SHIFT REGISTER AND LOGICAL CIRCUITS

1. Background

The use of magnetic cores as storage elements for digital computers was proposed by Forrester at MIT in 1951 [2]. Further work in the field of magnetic-core matrix memories and switching was done by Rajchman at RCA [10,11] and Papian at MIT [9]. Wang at Harvard [15], and later Sands [12,13] and Sims [14], investigated the design of magnetic-core shift registers. The performance of logical arithmetic operations with cores was covered theoretically by Guterman et al [5] and Minnick [7] while the requirements for a three-input core adder were investigated at the Naval Ordnance Laboratory, Corona [8].

2. Shift Register Design

It was first hoped to develop a shift register of the type shown in Figure 5 using only one core per bit of information and operating at about 300 Kc with one μsec pulses. This type of register, while capable of high operating speeds, tends to be somewhat critical in design due to the rather delicate time-energy relationships which must exist in the interstage delay network during transfer of information. This consideration and limitations on the number of turns which could be threaded on to the cores indicated the advisability of abandoning this particular approach in favor of the two-

cores-per-bit register illustrated in Figure 6 which it was felt could be more quickly brought to a state of satisfactory stable operation. It seems relatively certain that the above mentioned problems were not insurmountable and, had this been the predetermined major realm of endeavor, further investigations would have been made.

The operation of the shift register shown in Figure 6 is briefly as follows. Suppose initially core #1 is set to the "1" state, corresponding to the $+B_r$ position on the hysteresis loop of Figure 7, by pulsing the input winding as shown. All other cores are storing "0's", corresponding to the $-B_r$ position. Shift pulse "A" (see Figure 8) is applied to the shift winding of core #1 and all other odd numbered cores as well. In all these cores except #1 the mmf due to the current pulse merely pushes the core back along the loop and no appreciable flux change occurs. In core #1, however, the shift pulse causes a large flux change to occur as the loop is traversed from $+B_r$ to $-B_r$ which induces a negative voltage in the output winding. This signal passes through the series diode and the input winding of core #2 which it sets to the "1" state. The impedance relationships of output and input circuits must be such that the flux change in core #2 is completed before that occuring in core #1. Otherwise, once the first core has reached saturation no energy can be transferred through it to the second. No signal output from core #2 to #3 occurs during the above process because the signal is

of the wrong polarity to be passed by the series diode. The series resistor provides some degree of current regulation and impedance match necessary because the effective impedance of the input winding changes as the core switches from one state of magnetization to the other and, in addition, serves to prevent the input winding from acting as a "shorted turn" during re-set.

Now the "B" shift pulse (Figure 8) is applied to core #2 and all other even numbered cores. The "1" which was stored in core #2 is now advanced to core #3 in precisely the same manner as that described previously. No signal is fed back from core #2 to #1 because the output winding of core #1 is effectively by-passed by the shunt diode. Successive pairs of "A" and "B" pulses shift the information down the register at the rate of two stages, or one bit, per pair.[1]

The cores used in this investigation were chosen chiefly on the basis of their availability. They were a General Ceramics type having the following nominal characteristics:

Outside diameter	.375 inches
Inside diameter	.187 inches
Thickness	.125 inches
H_c	.65 oersteds
B_s	2000 gauss
B_r	1920 gauss

Sands, in an analysis which is both theoretical

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[1] The convention will be adopted of referring to each core and its associated circuitry as a stage.

and empirical, derives from energy considerations an expression for the equivalent input resistance of a core during switching by a current pulse [12]. The energy dissipated in the core is equal to the input energy minus the energy returned by the core at the end of the current pulse. For cores having a ratio of B_r/B_s of .95 or better the energy returned is less than 3% of the input energy and may be neglected. The input energy may be calculated from the dimensions of the hysteresis loop and a resistance found which will dissipate the same amount of energy during switching. Dividing this resistance by the square of the number of input turns, to make its application to design procedures more general, an equivalent resistance per turns squared, $\overline{R}_o$, is shown to be (using Sands' notation [13])

$$\overline{R}_o = \frac{A(B_r+B_s)\times 1.26\times 10^{-8}}{H_m T L} \qquad (2)$$

where A is cross sectional area of core in sq. cm.
B_r is residual flux density in gauss
B_s is saturation flux density in gauss
H_m is driving field in oersteds
T is switching time in sec.
L is mean flux path length in cm.

Substituting the previously listed core characteristics, after making the necessary units conversions,

$$\overline{R}_o = \frac{.076(1920+2000)\times 1.26\times 10^{-8}}{.65\times 5\times 10^{-6}\times 2.25}$$

$$= 0.51 \text{ ohms per turns squared.}$$

Choosing the ratio of unwanted to wanted flux transfer, F_{12}, to be 1/8 and assuming the forward resistance of the

diodes (1N34A's) to be about 100 ohms, the value of the series resistance, R_1, was found from the relationship

$$F_{12} = \frac{N_5 R_r}{N_7 (R_1 + R_r)} \qquad (3)$$

where N_5/N_7 is the turns ratio of input to output windings
R_r is the forward resistance of the diodes
R_1 is the series resistor.

Substituting in (3),

$$\frac{1}{8} = \frac{1}{2} \times \frac{100}{100 + R_1}$$

and $R_1 = 300$ ohms.

Now the number of turns required on the input winding can be determined from:

$$N_5^2 R_o = R_1 + R_r = 300 + 100 = 400 \text{ ohms} \qquad (4)$$

$$N_5^2 = \frac{400}{.51} = 783 \text{ turns squared}$$

$$N_5 = 28 \text{ turns on input winding} \qquad (5)$$

$$N_7 \geq 2N_5 \geq 56 = 60 \text{ turns on output winding.} \qquad (6)$$

3. Logical Circuit Design

The design of the logical circuits was, in general, less straightforward and well defined than that of the shift register. The bases for the design were the elementary logical operations defined by the truth tables contained in the summary of binary logic presented in Appendix I.

It has been shown [5] that three basic requirements are necessary to an all-core logical system, namely, 1. storage or delay, 2. amplification, and 3. two of

the three logical operations AND, OR, and NOT. That the first two requirements are implicitly satisfied by proper operation of the shift register may best be shown by considering the particular mode of operation of the register which was used for test and demonstration purposes, described later in Chapter VII, in which a single "1" is cycled continuously through the register.

Cores lend themselves well to use as OR gates since any one of two or more inputs can set a core to saturation. The OR circuit used was identical to an ordinary shift register stage except that an additional 28-turn input winding was provided as indicated in Figure 9.

Either AND or NOT operation could have been chosen for the second logical operation, but the latter seemed to be more useful for this application since the logical equations for addition are most often written in terms of the input functions and their complements or NOT's. Also, direct realization of an AND circuit with cores would be quite difficult if the inputs are derived directly from cores and the output must be able to switch the following core, as has been assumed throughout the system under consideration. A coincident-current core memory is essentially an AND device since an output is desired only from the core which lies at the intersection of the selected X and Y lines. Here, however, as in other previously proposed systems of cores, only a voltage output signal is desired for use as an input to the following circuit.

Minnick [7] proposes a one-level AND circuit with cores, but manipulation of his equations is instructive. Using his notation and definitions,

$$z' = 1-z \qquad \text{defined as inverse } z \qquad (7)$$

$$f_1(x_1,x_2) = x_1'x_2' \qquad \text{AND} \qquad (8)$$

$$y \oplus z = 1-y'z' \qquad \text{defined as inclusive OR} \qquad (9)$$

$$f_2(x_1,x_2) = x_1 \oplus x_2 \qquad \text{OR} \qquad (10)$$

From these definitions it must follow that

$$\begin{aligned} f_2(x_1,x_2) &= x_1 \oplus x_2 && (10) \\ &= 1-x_1'x_2' && \text{from } (9) \\ &= 1-f_1(x_1,x_2) && \text{from } (8) \\ &= f_1'(x_1,x_2) && \text{from } (7) \end{aligned}$$

and thus OR = AND' or AND NOT. This conclusion implicitly defines a logical structure other than that presented in Appendix I and which seems to offer no particular advantage for present purposes.

Complementation, which corresponds to the logical NOT, may be accomplished in more than one way. For instance, if a "1" were represented by a positive pulse then "$\overline{1}$" (NOT 1) might be a negative pulse, and vice versa for the "0". Complementation in this case might be accomplished rather easily with a couple of biased cores by properly arranging the sense of the various windings. Unfortunately, however, this is not the situation encountered here. The output of the magnetic-core shift register is such that "1" is represented by the presence of a pulse, normally negative in this system but dependent only on the sense

of the output winding, and "0" by the absence of a pulse. To complement this output the circuit shown in Figure 10(a) was used with operation to be as indicated in Figure 10(b). With no signal input, i.e., a "0" to be complemented, the externally generated clock, or shift, pulse drives "through" the bias and causes the core to switch from point "a", where it had been held by the bias current, to point "b" with a large resultant flux change and a negative output signal which is the desired "$\overline{0}$". If an input signal is present, i.e., a "1" to be complemented, this signal works against or inhibits the clock pulse, since they arrive coincidentally, to such a degree that the net mmf is zero or so nearly zero that the core remains essentially at "a", no appreciable flux change occurs, and no output signal is generated which is the desired "$\overline{1}$".

CHAPTER VI

ADDER DESIGN

To add the output of two registers in binary fashion it is necessary also to account for any carry which may have resulted from the previous addition of the next least significant binary digits. To perform all this simultaneously a three-input adder of the type shown in Figure 11 could be rather easily designed directly from the logical equations of Appendix I. Such an adder was built at the Naval Ordnance Laboratory, Corona, using DC sources as experimental inputs through toggle switches and it is reported to have operated satisfactorily with a S/N as high as 9:1 (on an amplitude, rather than area, basis). To achieve this result using as inputs the outputs of previous cores in the system is quite another matter, however, and even moreso if the output signal from the adder must itself be of sufficient magnitude to drive the next core in the system to saturation. Two possibilities were explored.

First consider asynchronous operation of the adder, that is, without benefit of shift pulse. This implies that the input pulses would have to be sufficiently large not only to set the core, but to shift the output to the next core as well. Also, since the adder cores must in some cases change state, unlike the "I" mode of operation, this will load the driving cores rather heavily. Further-

more, consider the relative states of magnetization of each core of the adder for all possible input conditions as shown in the table of Figure 12 which may be constructed directly from the logical equations. The significant outputs are encircled. Inspection of this table indicates that what might be termed four-step operation is required. If all cores were biased with a steady DC current to a relative state of "minus two" then a full output, sufficient to set another core to saturation, would be desired when a core is driven up through the bias with a relative drive of "three". This same core, however, is required under other circumstances to give no output for a drive of "two", and, worse still, the output of three such cores in series must still be negligible. Considering the possible variations in the shape of the input pulses from the various cores this seems unreasonable to ask.

The alternative procedure was to provide a shift pulse to each adder core and to operate it in somewhat the same manner as the NOT cores. In this way the input signal would have only to inhibit the shift pulse to the desired degree. This would eliminate the problem of loading the previous cores and at the same time provide an external source capable of supplying the power required to shift to the following core. The disadvantages to this scheme are twofold. First, the trouble encountered with only one inhibiting signal in the NOT cores quickly discourages the practice of piling three such signals, one

atop the other as it were, and expecting good discrimination or S/N. Second, considering that it had been established experimentally that approximately 100 turns were required on the input winding to inhibit properly, this would mean each adder core must have three 100-turn input windings, one 20-turn bias winding, one 20-turn shift winding, and one 100-turn output winding. This is just about twice as many turns as it is possible to thread by hand through the cores being used. This latter trouble, incidentally, would have hampered the previous scheme also and is the best immediate, single reason for not attempting the three-input adder.

The decision to proceed with a two-input adder, or essentially two half-adders, was a costly one in terms of operating speed.

The logical equations for a half-adder are:

$$\text{Sum} = (A+B)\cdot\overline{(A\cdot B)} \tag{11}$$

$$\text{Carry} = A\cdot B \tag{12}$$

Inspection of the truth tables of Figure 13 indicates that the AND operations can be eliminated by making the substitution:

$$A\cdot B = \overline{\bar{A}+\bar{B}} \tag{13}$$

Expanding the half-adder equations using this substitution,

$$\begin{aligned} \text{Sum} &= (A+B)\cdot\overline{(A\cdot B)} \\ &= (A+B)\cdot(\bar{A}+\bar{B}) \\ &= \overline{\overline{(A+B)}+\overline{(\bar{A}+\bar{B})}} \end{aligned} \tag{14}$$

$$\text{Carry} = A \cdot B$$
$$= \overline{\overline{A}+\overline{B}}$$

Although these equations appear distended and awkward they give promise of being more nearly physically realizable than the others.

The block diagram of a half-adder designed to implement the preceding equations is shown in Figure 14. Two half-adders of this sort may be combined with an OR gate in the manner shown in Figure 15 to form a full adder.

The system proposed by Minnick [7] achieves some saving in number of cores over that described above by accomplishing the complementing simultaneously with the OR operation in a single core. However, the complexity of the timing pulse schedule is considerably increased and the speed of operation would remain the same.

No consideration has been given to the problem of switching "one-out-of-many" using core matrices since it was not germane to the system proposed here and since the procedures have been well established in conjunction with the magnetic-core matrix memories previously mentioned [10,11].

CHAPTER VII

EXPERIMENTAL RESULTS

1. Shift Register

Two stages of the shift register were built using the design values specified in Chapter V. Experiments showed that these values did not give a satisfactory S/N so the number of turns on the output winding was increased, eventually to 100 turns before a really good S/N was obtained. At the same time the series resistor was optimized at 150 ohms. For these conditions the flux transfer ratio, F_{12}, was calculated from equation (3) to be:

$$F_{12} = \frac{28}{100} x \frac{100}{100+150} = .112$$

or a S/N of about 9:1 on an area, or flux, basis. Actually a S/N of about 20:1 was obtained in operation by driving the shift windings with a pulse of about 12 NI, ten µsec in duration (see Figure 16).

This discrepancy was puzzling at first, but further research into the literature provided a clue. In operation of a register somewhat similar to this one, although considerably faster, Sims at MIT found the effective forward resistance of 1N34A diodes to be about 30 ohms instead of the 100 ohms assumed [14]. Substituting this value for R_T in equation (3),

$$F_{12} = \frac{28}{100} x \frac{30}{30+150} = \frac{28}{600} = .046$$

or a S/N of 21.4 which is in good agreement with the results of rough graphical integration of the oscilloscope photograph traced for Figure 16.

A ten-stage, five-bit register was built and tested using this design except that the number of turns on the shift winding was increased from 15 to 20 to ease the load on the current driver. This register was eventually split into two-five-stage registers, later designated "A" and "B", for further testing and experimental purposes.

The test procedure for the shift register fell into three categories: first, to determine whether the register operated correctly under normal circumstances; second, to determine its storage and attenuation or amplification characteristics; and third, to investigate the limits of reliable operation.

The first function was easily satisfied by programming various sequences of "1's" and "0's" into the first stage from the Magnetic Circuit Tester described in Chapter IV and checking the output with an oscilloscope.

The second type of test was a more exacting one. With no shift pulses applied, the first core was set to the "1" state using an external unidirectional current source, which was then removed. All other cores were storing "0's". The output of the tenth (last) stage was then connected to the input of the first stage and shift pulses were applied to the shift windings. The "1", initially stored in the

first stage, was successively propagated down the register and caused to recycle itself indefinitely, "biting its own tail". No attenuation of the signal nor deterioration in S/N as a function of time occurred, implying the theoretical possibility of building a shift register having an infinite number of stages.

To determine the limits of reliable operation of the register, the mode of operation just described was used while the shift pulses were reduced in duration and amplitude. In this way the "worst possible" condition, sometimes specified in computer tests, was achieved since failure in any stage would cause the single bit being circulated to be lost. In this way it was found that the minimum tolerable shift pulse duration was about 5.0 µsec and the minimum amplitude about 10.8 NI and each was relatively independent of the other.

It is interesting to note that failure occurred in a different way when the pulse amplitude was reduced below its minimum than when the pulse duration was reduced too far. When the amplitude was reduced below 10.8 NI the single "1" being recirculated disappeared. This is felt to result from the shift pulse being of insufficient magnitude to transfer to the next core the energy necessary for a complete flux change. This loss is then reflected in the next stage and within a few cycles the cumulative effect reduces the flux change to that of the noise level and,

by definition, the register contains all "0's".

The effect of reducing the pulse duration below five µsec was to cause the register to fill with "1's". This behavior is explained on the basis that the core from which the "1" is being shifted does not have time to complete its flux excursion along a major loop and hence comes to rest at a point above $-B_r$. Further shift pulses occurring before the re-arrival of the "1" tend to drive the operating point toward $-B_r$ and each of these minor excursions can be thought of as transfering some flux to the following stage. Eventually this flux build-up in succeeding stages of the circle of operation will amount to storage of a "1" in every stage. It is to be noted that at least one "1" must be present in the register for this chain of events to take place. A register filled with "0's" will never spontaneously fill with "1's" as the pulse width is reduced.

This completed the test of the register which was, for the purposes of this project, only a means to an end. For this reason design refinements which might have been investigated further had time permitted were ignored. Further experience has indicated that improvements might be made in the direction of reducing the shift pulse amplitude, and perhaps duration, by making the turns ratio more nearly 2:1, the theoretical optimum, and at the same time increasing the value of the series resistor in each stage.

It is doubtful, however, if too much can be accomplished without some deterioration in S/N and sacrifice in stability of operation.

2. Logical Circuits

The logical OR gate functioned as predicted and no modifications were necessary.

The complementing, or logical NOT, circuit showed an unsatisfactory S/N when first tested and the trouble was traced to the "I" function.

The shift pulse supplied to the complementing core was originally made identical with the shift pulse which had shifted the information to be complemented out of the preceding core. Since, however, the flux change in the first core is completed before the shift pulse is removed, and, in fact, is completed in about the first six µsec of a ten µsec shift pulse, a condition somewhat as shown in Figure 17 results where the shaded area roughly represents the uncanceled mmf. This leads to an unwanted output for "I" occurring during the latter half of the shift pulse. For this reason the width of the shift pulse to the complementing core was reduced to about five µsec and was increased slightly in amplitude over the normal shift pulses to help overcome the 1.10 NI DC bias. At first the input signal amplitude was found to be insufficient to inhibit the shift pulse which itself had to be great enough when uninhibited to switch the complementing core and to drive

the following core to saturation. This difficulty was overcome by winding 100 turns on the input instead of the usual 28. This was possible here because the loading effect on the preceding core is negligible during the subtraction of the mmf's since no traversal of the hysteresis loop occurs. Because it was difficult to observe the output of such a low impedance circuit directly, the output was made to set a shift register stage and the output of this latter core, observed across the normal 150 ohm load, had a S/N of about 20:1 for the complemented output. It is quite possible that a gain in S/N occurred in the intermediate core since such a phenomenon was observed in the shift register. Still, the observation of S/N at the output of the next stage seems to be a fair criterion since this turns out to be the way in which the circuit is used in the system.

The half-adder of Figure 14 which is shown schematically in Figure 18 was actually constructed and tested. Operation was only partly successful in that the upper branch, or "straight through" part of the circuit, functioned correctly for several stages while the lower, or complementing, branch did not. It was apparent that the interaction of the various cores on one another was considerable even though isolating diodes had been provided between all stages and a high-impedance DC bias source was built to replace the ignition batteries used previously.

Further isolation was necessary and, again, the price to be paid was time and an increased number of components. Buffer stages, which were normal shift register stages, were inserted in the half-adder as indicated in Figure 19. Also shown is the increase in time spent in the half-adder by a factor of three. In an actual computer this would be a very serious limitation but for the purposes of this study it was an undesirable but acceptable condition.

CHAPTER VIII

CONCLUSIONS, RECOMMENDATIONS, AND POSSIBILITIES

1. Conclusions

The investigations reported in this thesis seem to indicate that an all-core computing system is possible. The basic circuits for such a system have been designed and tested. Lack of sufficient current pulse sources, coupled with lack of time, precluded building and testing the entire system. However, using only combinations of circuits which were proven successful, the block diagram of Figure 20 represents the fulfillment of all the requirements for the basic computer system proposed in Chapter II. It appears that the proposed system could be operated at a basic repetition rate of 50 Kc in the logical portion, i.e., the adder, and thus one-third this rate in the shift register. This implies that the serial addition of n binary digits could be accomplished in (n+2) times 60 μsec which compares favorably with many modern machines.

The basic speed limitation in the system is the time required in the second half-adder to determine the secondary carry digit and feed it back through the OR gate to combine with the partial carry from the first half-adder, all this is time to add to the partial sum due to the next most significant digits. To accomplish this the shift register operates at only one-third the pulse rate of the adder and various timing delays have been introduced

to insure arrival of the information at the proper place at the proper time. The recirculation of the contents of the "A" register must also be delayed a time equal to that spent in the adder.

The entire system, including two ten-bit shift registers and the adder, uses the following components:

Cores	84
Diodes	158
Resistors	74

The vacuum tube equivalent, using a three-input tube adder, would require something in the neighborhood of 33 tubes.

The maximum reliable rate of operation of the core system would be about 15 to 20 Kc, that of a comparable system using tubes in the range of 100 Kc.

From the power requirements computed in Chapter III, and assuming ten µsec shift pulses for operation at 16.7 Kc, the power consumed will be less than

$$11.5\text{x}10^{-6}\text{x}16.7\text{x}10^{3}\text{x}84 = 16.1 \text{ watts}$$

This does not include whatever power may have been necessary to generate the shift pulses nor any losses in the DC bias supply. The vacuum tube system would probably draw in excess of 100 watts.

It appears that compared to its vacuum tube counterpart this system would be more complex and slower but use less power. The real advantages of the core system, though, are felt to be its reliability and ruggedness. Commercially available magnetic-core shift registers now use one core

per bit and one diode per stage. This single improvement in the shift register alone would reduce the diode count below 100 and the cores to 64. Further improvements in design, materials, and techniques may be expected to correspondingly brighten the core picture, all without sacrificing the prime advantages of cores -- high reliability and long life.

2. Recommendations

The possibility of improving the shift register design was discussed briefly in Chapter VII and some general recommendations were made toward that end.

In the logical circuits improvements would be desirable to reduce the time spent in the adder and to reduce the complexity. The first step might be in the direction of eliminating the buffer stages in the half-adders and the second step to eliminate the half-adders altogether in favor of a three-input or full adder.

The possibility exists that unforseen combinative difficulties might arise in the actual testing of the system proposed in Figure 20 should it be constructed in its entirety. In such a case additional buffer stages could be inserted as necessary, keeping always in mind the associated reduction in operating speed. The ability of a single core to set two cores in a branch circuit has been experimentally verified.

3. Possibilities

Considerable feeling exists among some engineers that the future of computers lies largely in machines willing to sacrifice some speed of operation for reliability. An example often cited is the fable of The Tortoise and the Hare. Perhaps a better analogy is that of the very fast but expensive and tempermental race horse which must be carefully groomed only to spend a few minutes on the track at high speed while the ordinary work horse can be expected to be in top form nearly all the time and to perform its duties for long periods without special handling. The all-magnetic computer may well be the work-horse of the future.

Other impending developments use cores in more conventional machines. Designers have in the planning stages a system to utilize complex, yet highly reliable, switching circuits to speed computer operation. One method visualizes a "vertical shift" to any one of a series of magnetic-core switch lines which may perform such functions as "shift right one place", "shift left two places", "shift to output", etc.

Further logical, or arithmetic, operations could be speeded by the use of function tables which might consist of core matrices whose reading windings follow a certain pattern. For example, consider the possibility of a direct decimal multiplier. A square core matrix having ten

X-inputs and ten Y-inputs would have one or two cores at the intersection of each X and Y line. The reading windings of these cores would be arranged in such a manner as to give the product of X and Y. For instance, at the intersection of the X=7 and Y=4 lines are two cores. Through one is threaded an output winding connected to the terminal corresponding to "8", through the other the "carry 2" output winding. Simultaneous half-excitations, of the type used in coincident-current matrix memories, when applied to the X=7 and Y=4 inputs would induce output voltages only in the "8" and "carry 2" lines.

As a further example of the use of function tables, consider a ten-by-ten matrix having three sets of reading windings laced as shown in Figure 21. In this case the matrix would perform the function of comparison of the numerical magnitudes of the inputs, the outputs being "X is greater than Y", "X is equal to Y", or "X is less than Y".

If the preceding examples seem to involve a relatively large number of cores this is no accident. Preliminary investigations of the possibility of incorporating extensive core logic into a computer have been made by International Telemeter Corporation. The conclusion was that cores are practical as a replacement for tubes as logical elements at present only when large "swatches" of logic are to be performed in parallel. The advent of power transistors, capable of supplying the relatively large

driving currents used in core work, is expected to lend impetus to the use of cores as logical elements in computers.

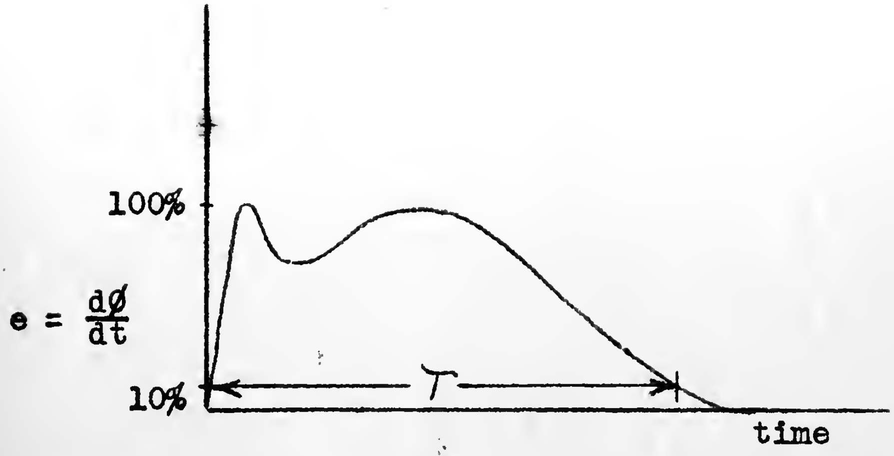

Figure 1. Voltage output from switched core

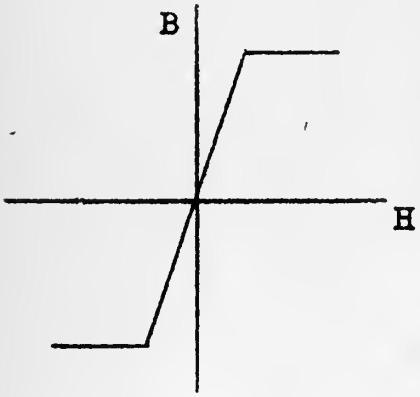

Figure 2. Idealized slant hysteresis loop

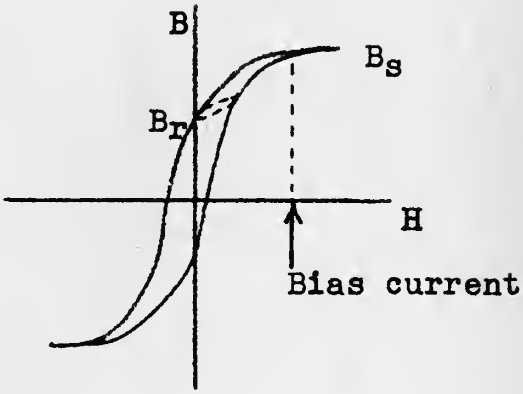

Figure 3. Operating conditions on slant-loop core

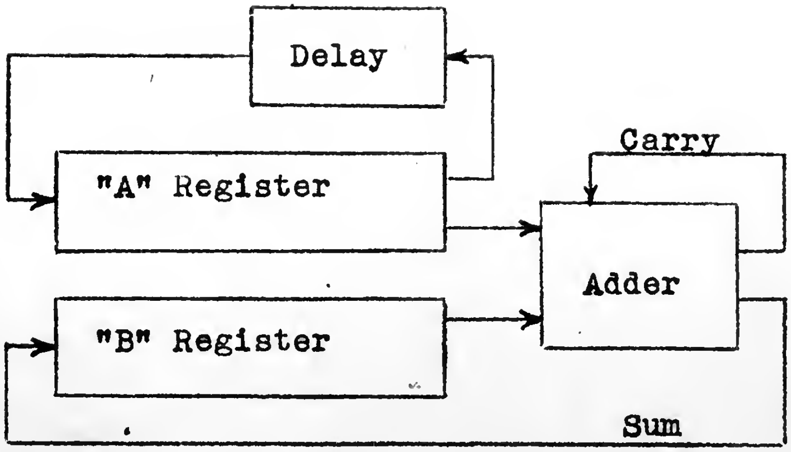

Figure 4. Proposed magnetic-core arithmetic unit

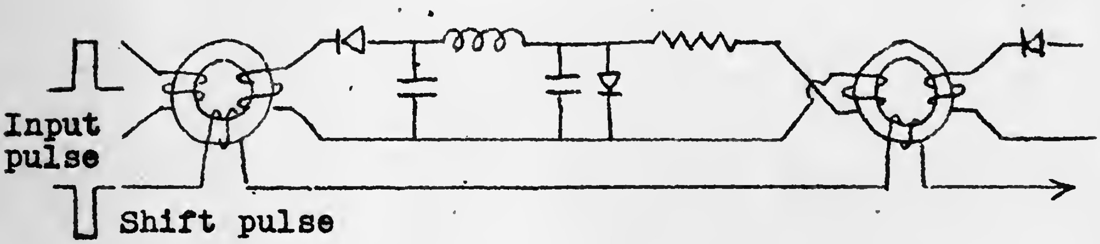

Figure 5. Basic form of one-core-per-bit shift register

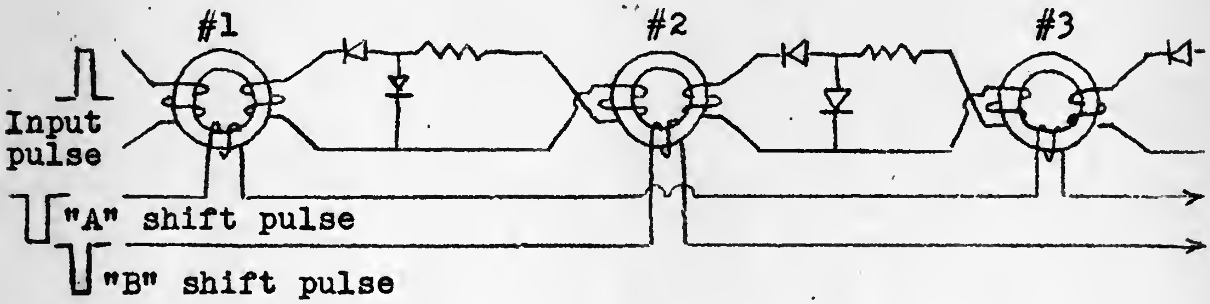

Figure 6. Basic form of two-cores-per-bit shift register

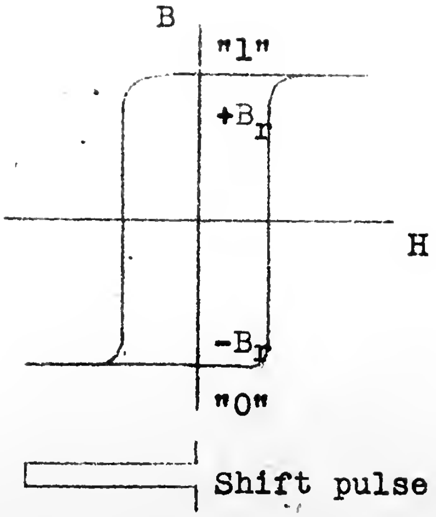

Figure 7. Idealized square hysteresis loop of ferrite core

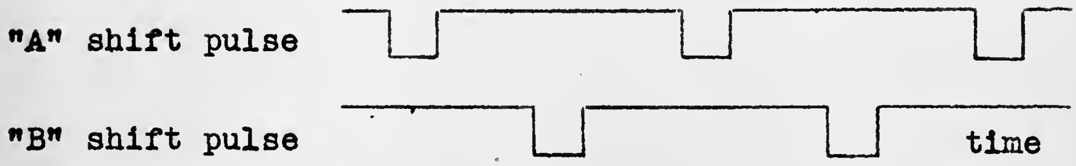

Figure 8. Time relationship of "A" and "B" shift pulses

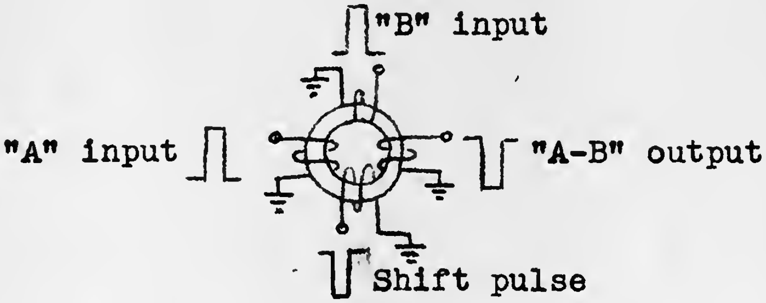

Figure 9. Logical OR circuit

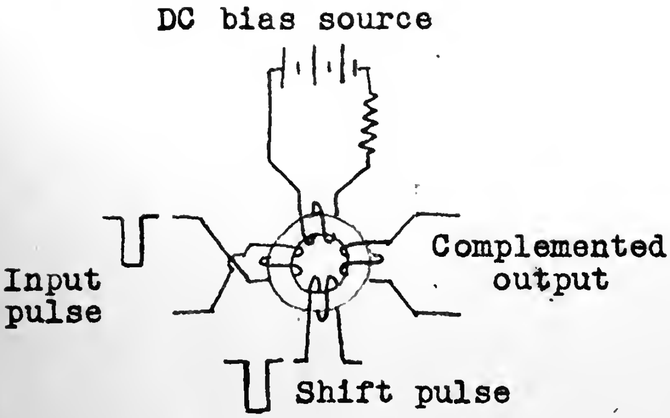

Figure 10a. Logical NOT circuit

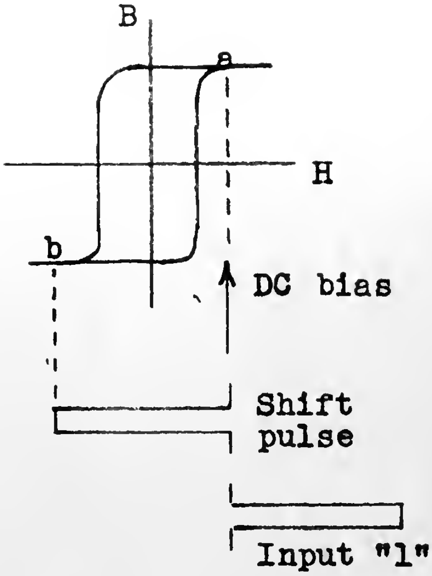

Figure 10b. Operation of logical NOT circuit

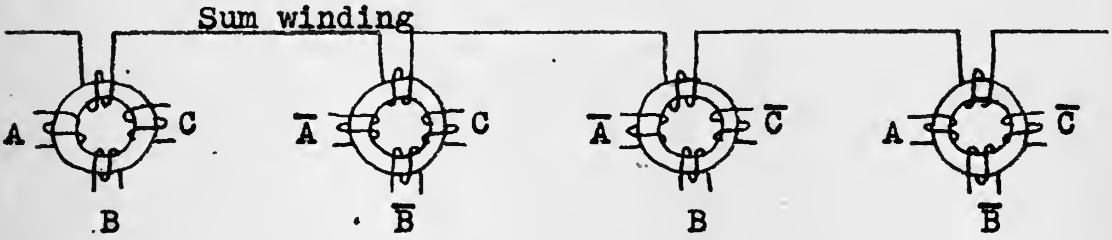

Figure 11a. Sum output of three-input adder

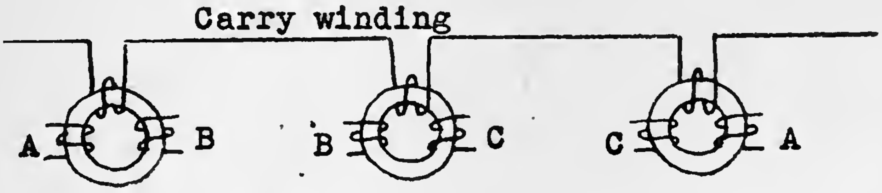

Figure 11b. Carry output of three-input adder

Input			Relative state of magnetization of core				Desired sum output
A	B	C	#1	#2	#3	#4	
0	0	0	⓪	2	2	2	0
0	0	1	1	③	1	1	1
0	1	0	1	1	③	1	1
0	1	1	2	2	2	⓪	0
1	0	0	1	1	1	③	1
1	0	1	2	2	⓪	2	0
1	1	0	2	⓪	2	2	0
1	1	1	③	1	1	1	1

Figure 12. Relationships existing in three-input adder of Figure 11a.

A	B	$\bar{A}$	$\bar{B}$	$A \cdot B$	$\bar{A}+\bar{B}$	$\overline{\bar{A}+\bar{B}}$
0	0	1	1	0	1	0
0	1	1	0	0	1	0
1	0	0	1	0	1	0
1	1	0	0	1	0	1

Figure 13. Truth table

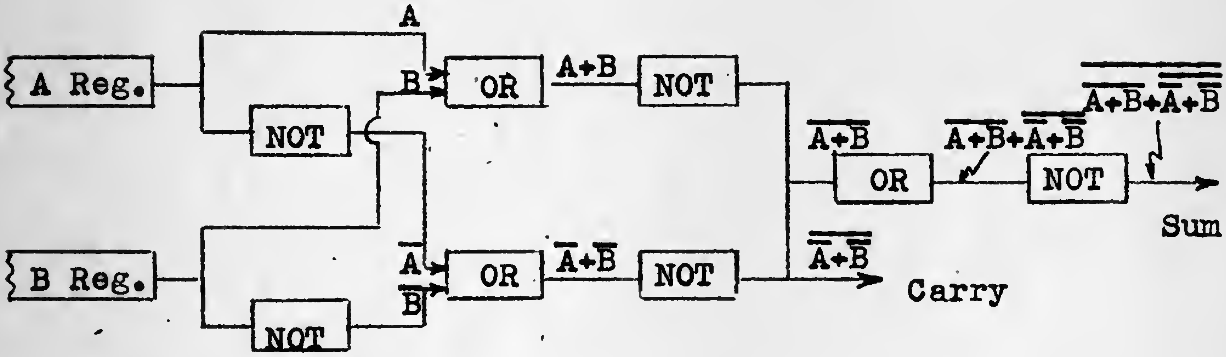

Figure 14. Block diagram of modified half-adder using only OR and NOT circuits

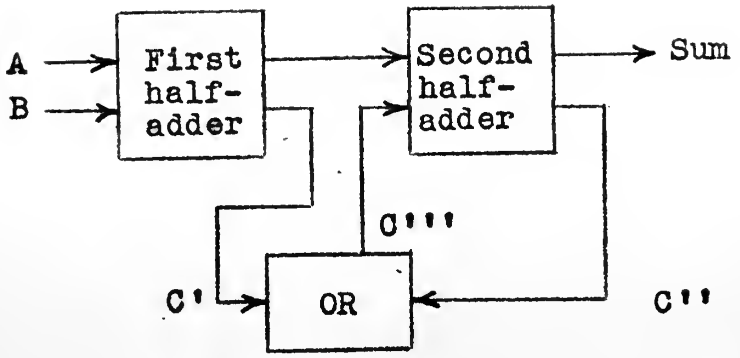

Figure 15. Block diagram of full adder

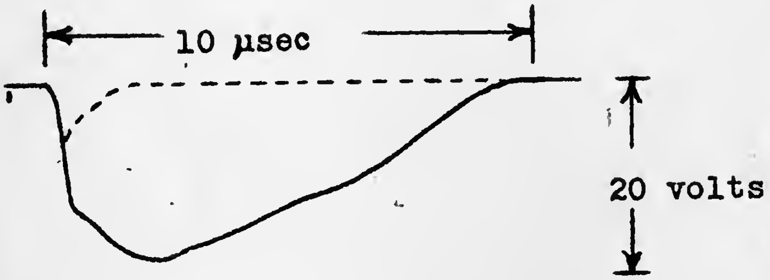

Figure 16. Tracing of oscilloscope photo of output pulse at last stage of shift register showing S/N

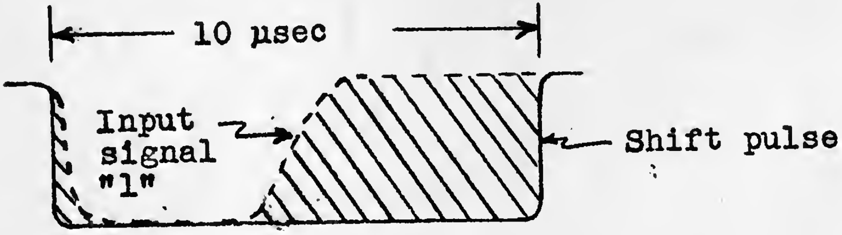

Figure 17. Current pulse conditions in complementing circuit

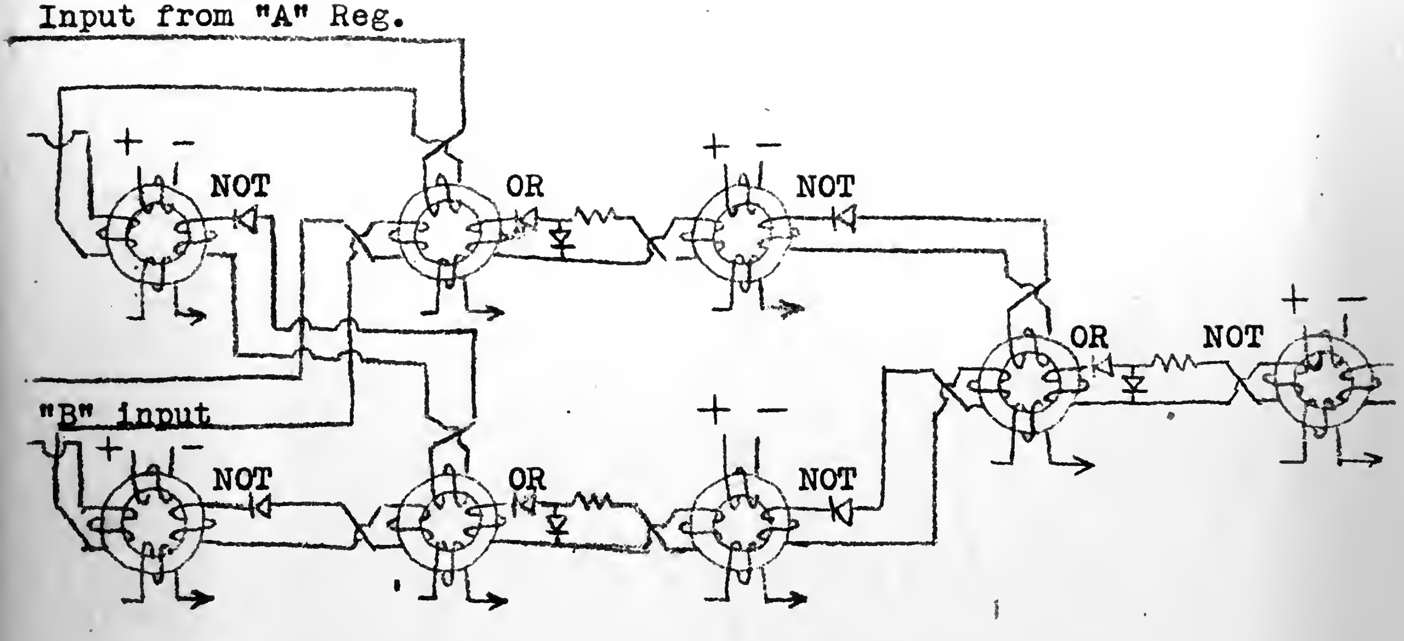

Figure 18. Schematic diagram of modified half-adder

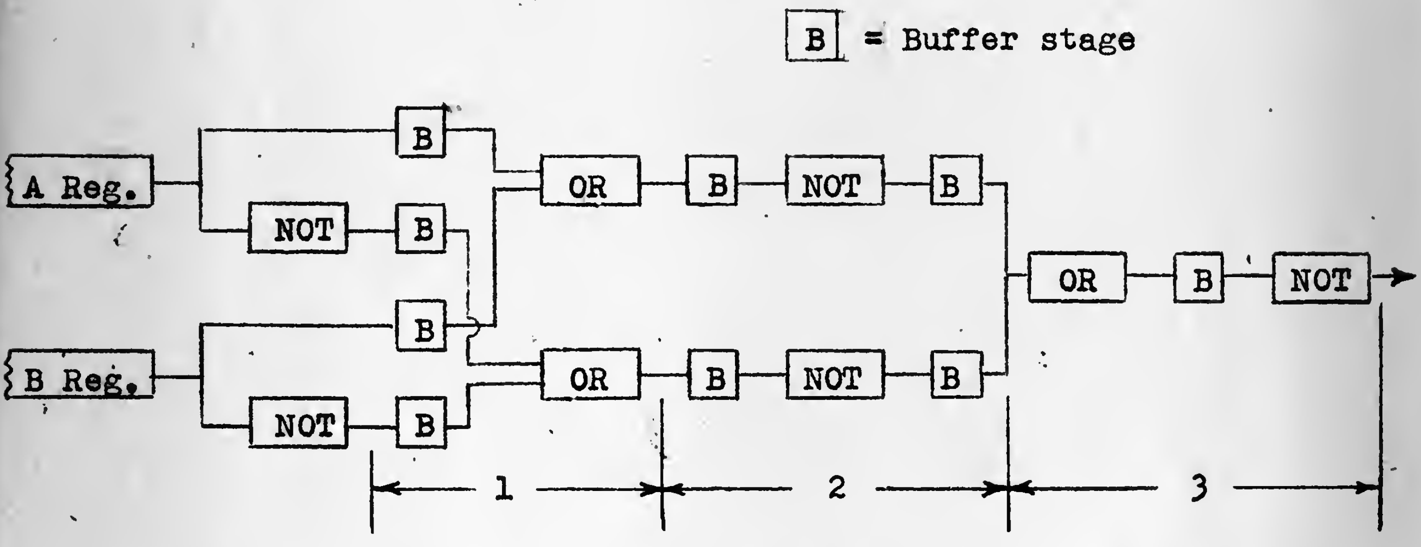

Figure 19. Block diagram of buffered half-adder showing number of clock times spent in passage of a digit

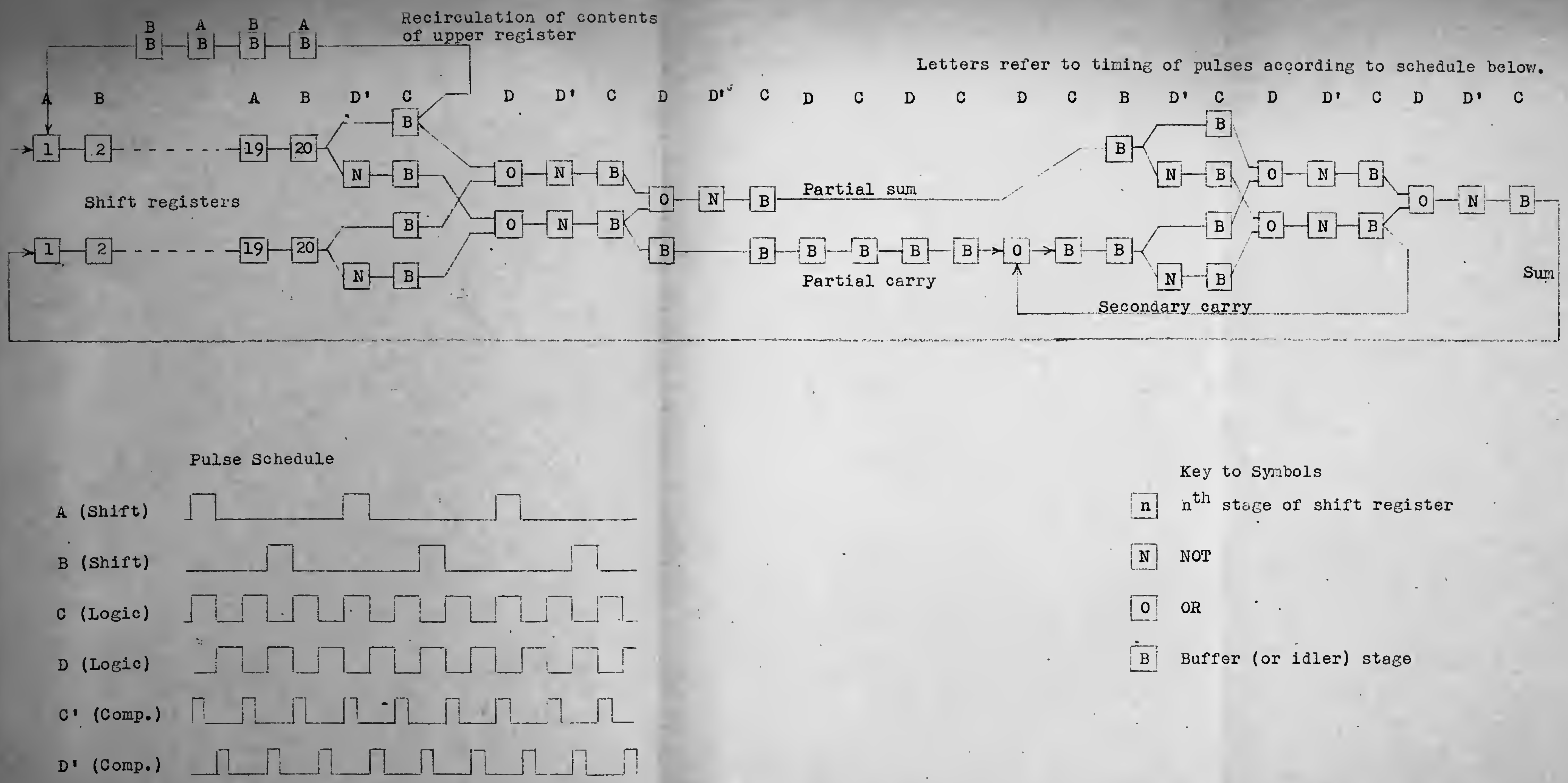

Figure 20. Block diagram of computer arithmetic unit using magnetic cores

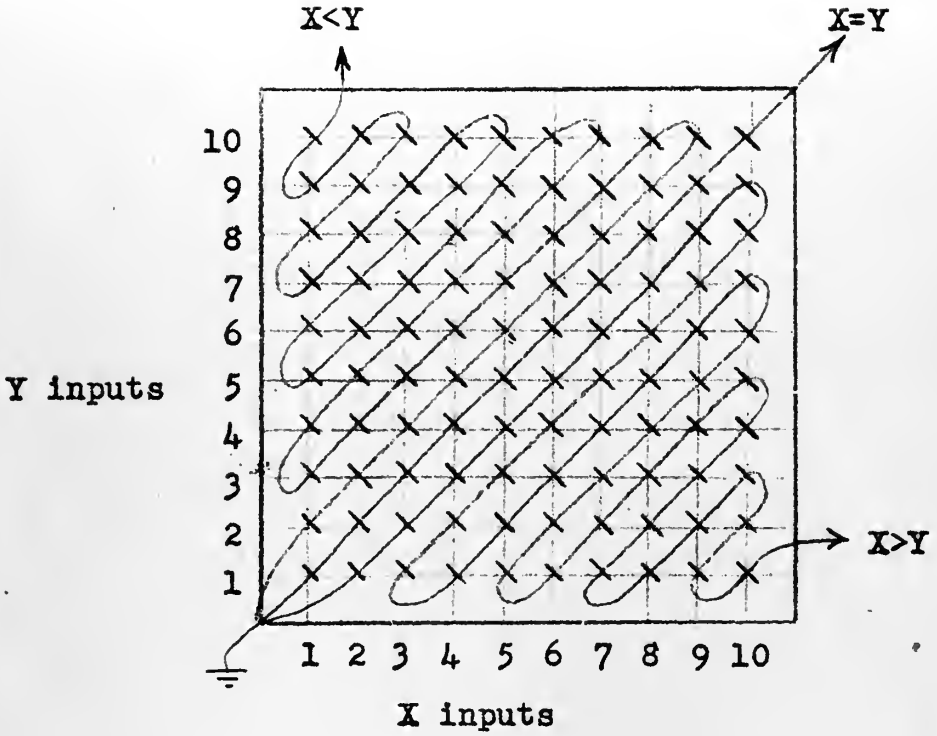

Figure 21. Function table for comparison of X and Y

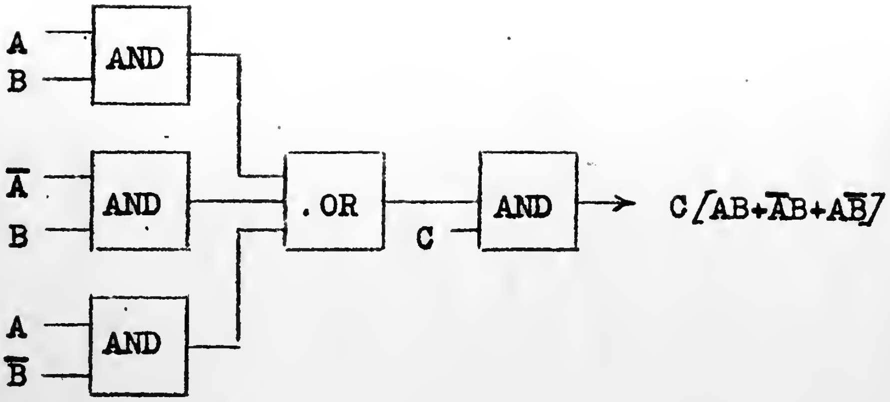

Figure 22a

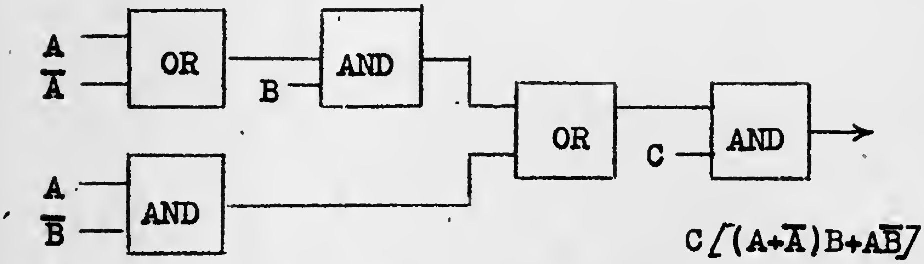

Figure 22b

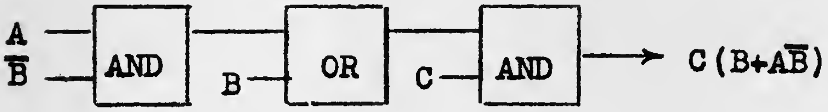

Figure 22c

Figure 22d

Figure 22. Various forms of logical equations

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Appendix I

BINARY LOGIC

I. General logical operations

A. OR (logical sum) - An output occurs when either one or both of two inputs, A and B, are present. This is symbolically written as A+B.

B. AND (logical product) - An output occurs only when both of two inputs, A and B, are present. This is written A•B.

C. NOT (logical complement) - An output occurs when its corresponding function is not present at the input. The output is called the "complement" or "prime" of the input function and is written (for an input A) as $\bar{A}$.

II. Truth tables

A. General logical operations

A	B	A+B	A•B	$\bar{A}$	$\bar{B}$
0	0	0	0	1	1
0	1	1	0	1	0
1	0	1	0	0	1
1	1	1	1	0	0

B. Two-input adders

A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

C. Three-input adders

A B C	Sum	Carry	Sum equation	Carry equation
0 0 0	0	0	ABC	AB(or others)
0 0 1	1	0	$\overline{AB}C$	AB "
0 1 0	1	0	$\overline{A}B\overline{C}$	AB "
0 1 1	0	1	ABC	BC
1 0 0	1	0	$A\overline{BC}$	AB "
1 0 1	0	1	ABC	AC
1 1 0	0	1	ABC	AB
1 1 1	1	1	ABC	AB "

Discarding the redundancies,

$$\text{Sum} = ABC+\overline{AB}C+\overline{A}B\overline{C}+A\overline{BC}$$

$$\text{Carry} = AB+BC+CA$$

D. Logical Identities

$$A+\overline{A} = 1$$
$$A\cdot\overline{A} = 0$$

$$(\overline{A+B}) = \overline{A}\cdot\overline{B}$$
$$(\overline{A\cdot B}) = \overline{A}+\overline{B}$$

$$A(\overline{A}+B) = A\cdot B$$
$$A+\overline{A}\cdot B = A+B$$

By using these logical identities of Boolean algebra the arithmetic of switching or gating operations may be expressed in several different ways. The choice in any particular application usually depends largely upon the physical or electrical realization of the specified operation, i.e., how many levels of logic can be tolerated from timing considerations, how many components must be used, what sort of load will be imposed on the driving circuit, etc.

As an illustrative example consider the simple

equation

$$(A+B)C$$

which is defined by the truth table which follows:

A B C	(A+B)C	Corresponding term for logical equation
0 0 0	0	ABC
0 0 1	0	ABC
0 1 0	0	ABC
0 1 1	1	$\overline{A}BC$
1 0 0	0	ABC
1 0 1	1	$A\overline{B}C$
1 1 0	0	ABC
1 1 1	1	ABC

The first logical equation results from considering simultaneously all three inputs and writing the corresponding terms of the equation by inspection of the truth table, complementing the inputs as necessary to give the desired output upon multiplication. After discarding the redundant terms the result is:

$$(A+B)C = ABC+\overline{A}BC+A\overline{BC}$$

The multiplication together of the three inputs A, B, and C, in each term implies some sort of triple coincidence gate which is generally difficult to achieve physically. Hence the equations may be manipulated to a more usable form. For each step a block diagram of the corresponding circuit is given and the relative complexity, as determined by the number of gates used, and the number of logical levels are indicated.

Form of logical equation	Block diagram Figure	Relative complexity	Logical levels
$(A+B)C = C[AB+\bar{A}B+A\bar{B}]$	22a	5	3
$= C[(A+\bar{A})B+A\bar{B}]$	22b	5	4
$= C(B+A\bar{B})$	22c	3	3
$= C(A+B)$	22d	2	2

This final result, as might be expected, is the original equation.

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